

L Number	Hits	Search Text	DB	Time stamp
12	238	interposer and dicing and (chip or substrate or wafer)	USPAT; US-PPGPUB	2003/06/20 17:09
13	120	(interposer and dicing and (chip or substrate or wafer)) and @ad<=20001002	USPAT; US-PPGPUB	2003/06/20 17:18
14	89	((interposer and dicing and (chip or substrate or wafer)) and @ad<=20001002) and test\$3	USPAT; US-PPGPUB	2003/06/20 16:25
15	14	interposer and dicing and (chip or substrate or wafer)	EPO; JPO; DERWENT; IBM_TDB	2003/06/20 17:09
16	5	jerry near2 kline	USPAT; US-PPGPUB	2003/06/20 17:16

	U	I	Document ID	Issue Date	Pages	Title	Current OR
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20020097063 A1	20020725	9	Wafer level interposer	324/765
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6537831 B1	20030325	18	Method for selecting components for a matched set using a multi wafer interposer	438/14
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6483330 B1	20021119	18	Method for selecting components for a matched set using wafer interposers	324/754
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6483043 B1	20021119	12	Chip assembly with integrated power distribution between a wafer interposer and an integrated circuit chip	174/262
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6392428 B1	20020521	8	Wafer level interposer	324/755

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1			Kline, Jerry D.	<input checked="" type="checkbox"/>	<input type="checkbox"/>					
2	438/106; 438/107		Kline, Jerry D.	<input checked="" type="checkbox"/>	<input type="checkbox"/>					
3	324/158.1; 324/757; 324/765; 438/17; 438/18		Kline, Jerry D.	<input checked="" type="checkbox"/>	<input type="checkbox"/>					
4	174/260; 361/601; 361/794		Kline, Jerry D.	<input checked="" type="checkbox"/>	<input type="checkbox"/>					
5	257/E21.52 5; 257/E23.06 7; 324/158.1; 324/754		Kline, Jerry D. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>					

	<input type="checkbox"/>	<input checked="" type="checkbox"/> [1]	Document ID	Issue Date	Pages	Title	Current OR
1	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US A1 20020011663	20020131	39	FACE-UP SEMICONDUCTOR CHIP ASSEMBLIES	257/734
2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US B1 6498387	20021224	11	Wafer level package and the process of the same	257/620
3	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US B1 6489678	20021203	9	High performance multi-chip flip chip package	257/723
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US B1 6432744	20020813	16	Wafer-scale assembly of chip-size packages	438/108
5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US B1 6392306	20020521	41	Semiconductor chip assembly with anisotropic conductive adhesive connections	257/783
6	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US B1 6372527	20020416	43	Methods of making semiconductor chip assemblies	438/15

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1			Khandros, Igor Y. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>					
2	257/612; 257/678; 257/753		Yang, Wen-Ken	<input checked="" type="checkbox"/>	<input type="checkbox"/>					
3	257/666; 257/693; 257/737; 257/E23.02 6		Joshi, Rajeev	<input checked="" type="checkbox"/>	<input type="checkbox"/>					
4	438/118; 438/612; 438/616		Amador, Gonzalo et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>					
5	257/784		Khandros, Igor Y. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>					
6	257/E21.51 1; 257/E21.60 6; 257/E21.70 5; 257/E23.01 9; 257/E23.06 1; 257/E23.06 5; 257/E23.06 6; 257/E23.06 7; 257/E23.12 4; 257/E23.13 ; 257/E25.02 9; 438/113; 438/125		Khandros, Igor Y. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>					

	U	1 [1]]	Document ID	Issue Date	Pages	Title	Current OR
7	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6281046 B1	20010828	9	Method of forming an integrated circuit package at a wafer level	438/113
8	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6032356 A	20000307	39	Wafer-level test and burn-in, and semiconductor process	29/843

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
7	257/738; 257/778; 257/E21.50 3; 257/E21.50 8; 257/E23.06 5; 257/E23.12 4; 438/108; 438/615; 438/616		Lam, Ken M.	<input checked="" type="checkbox"/>	<input type="checkbox"/>					
8	257/E21.50 3; 257/E21.50 8; 257/E21.50 9; 257/E21.51 1; 257/E21.51 2; 257/E21.51 9; 257/E21.52 5; 257/E23.02 1; 257/E23.02 4; 257/E23.06 8; 257/E23.07 8; 257/E25.01 1; 257/E25.02 9; 29/842; 29/874; 324/756; 439/56; 439/591; 439/66		Eldridge, Benjamin N. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>					

	U	1 [1]]	Document ID	Issue Date	Pages	Title	Current OR
9	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5998228 A	19991207	39	Method of testing semiconductor	438/15

	Current XR f	Retrieval Classif	Inventor	S	C	P	2	3	4	5
9	228/179.1; 257/E21.50 3; 257/E21.50 8; 257/E21.50 9; 257/E21.51 1; 257/E21.51 2; 257/E21.51 9; 257/E21.52 5; 257/E23.02 1; 257/E23.02 4; 257/E23.06 8; 257/E23.07 8; 257/E25.01 1; 257/E25.02 9; 324/754; 324/762; 428/601; 428/620		Eldridge, Benjamin N. et al.	☒	<input type="checkbox"/>					

	U	1 [1]]	Document ID	Issue Date	Pages	Title	Current OR
10	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5832601 A	19981110	39	Method of making temporary connections between electronic components	29/843

	Current XRef	R trieval Classif	Inventor	S	C	P	2	3	4	5
10	257/620; 257/665; 257/E21.50 3; 257/E21.50 8; 257/E21.50 9; 257/E21.51 1; 257/E21.51 2; 257/E21.51 9; 257/E21.52 5; 257/E23.02 1; 257/E23.02 4; 257/E23.06 8; 257/E23.07 8; 257/E25.01 1; 257/E25.02 9; 29/840; 438/14; 438/18		Eldridge, Benjamin N. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>					